Objective:

The objective of this experiment is to design an active mirror circuit and load the mirror circuit to observe mirror circuit performance in different loading condition.

Circuit Diagram:

 

Fig 01: Schematic Diagram of the MOSFET current mirror circuit with load RL

Experimental Setup:

1.CD4007 IC – 1pcs

2.Resisrtor(1k-2pcs,3.3k-1pc,4.7k,1pc,10k-1pc)

Procedure:

First we have to measure the value of the resistors. Then we have to setup the circuit with proper connection. Then we have to take the measurements of the variables of the table of datasheet. Then we have to repeat the process of measurement by changing the values of the resistors. Finally we have to plot the characteristics curve of the MOSFET.

Measurements:

Part 01: Program of the referenced current mirror circuit:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  RL ohm |  R2 ohm |  VR1 (V) |  VR2 (V) | Iref=IR1=VR1/R1mA | IR2=VR2/R2 mA |
|  1k | 0.98k |  1.7V |  1.6V |  1.7mA |  1.63mA |
|  3.3k | 0.98k |  2.3V |  0.68V |  0.7mA |  0.69mA |
|  4.7k | 0.98k |  2.44V |  0.52V |  0.53mA |  0.53mA |
|  10k | 0.98k |  2.7V |  0.27V |  0.027mA |  0.28mA |

Part 02: Effects of the current mirror circuit by the load:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  Ra Ω |  RL=Ra+ R2 Ω |  VRL (V) |  IRL=VRL/RL mA |  VD\_Q2  (V) |
|  0 |  0.98k | 0.49V |  0.5mA |  4.48V |
|  3.3k | 4.29k |  2.1V |  0.49mA | 2.85V |
|  4.7k |  5.59k |  2.71V |  0.49mA |  2.24V |
|  10k |  11k | 4.6V |  0.42mA |  0.36V |
| 14.7k |  15.88k |  4.78V |  0.30mA |  0.18V |
|  25k |  25.9k |  4.85V |  0.18mA |  0.11V |

Answer to the question no:1

Measurement of necessary data using PSpice simulation:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Ra(Ω) | RL=Ra+R2(Ω) | VRL | IRL | VD\_Q2 |
| 0 | 0.98k | 0.18V | 0.172mA | 4.81V |
| 3.3k | 4.29k | 0.74V | 0.172mA | 4.26V |
| 4.7k | 5.59k | 0.968V | 0.172mA | 4.03V |
| 10k | 11k | 1.77V | 0.163mA | 3.21V |
| 14.7k | 15.88k | 2.36V | 0.149mA | 2.64V |
| 25k | 25.9k | 3.12V | 0.120mA | 1.88V |

MATLAB plotting code:

clear all

VD\_Q2=[4.48,2.85,2.24,0.36,0.18,0.11];

IRL=[0.5,0.49,0.49,0.42,0.30,0.18];

plot(VD\_Q2,IRL);hold on ;

VDx\_Q2=[4.81,4.26,4.03,3.21,2.64,1.88];

IRLx=[0.172,0.172,0.172,0.163,0.149,0.120];

plot(VDx\_Q2,IRLx);

 Plot 01: Plot of ID vs V\_DS using experimental data and PSpice simulated data

In the lab measured data, we can observe a dramatic change in the curve. But the PSpice gives us a very smooth curve. The fact is that, the real world devices are a little bit far from the simulation.

Answer to the question no:2

Operating temperature range: -40®C to +85®C

Number of MOSFET:06

There are two types.

Three N-MOS and three P-MOS.

Answer to the question no:3

The meaning of min is the minimum level and max means maximum level and typ means the typical value.

For example,low level of output voltage has typ=0 and max=0.01. That means, the typical value of the low level of output voltage is supposed to ve zero. But it can be 0.01 at maximum.Similarly to other parameters, min ,typ and max value applied.

Answer to the question no:4

The output current decreases with the increase of resistance between the drain terminal and the input voltage terminal. When the resistor value increased, the nmos operate in active mode

Conclusion:

 From this particular experiment, we have learnt that in a current mirror circuit the output current follows the reference current. That is why it is called current mirror circuit. We have also done the same experiment with loads and observed the Id\_VDS curve for transistor Q2. Finally, We have found the characteristic curve of MOSFET . There are very much difference between the measured values and pspice simulated values.