**Dept. of EEE, EWU, Summer 2014**

Course Name : Digital Logic Design

Course Code : EEE205

Experiment No : 01

Name of the Experiment : TTL/CMOS Logic and Switching Characteristics of

 Basic Logic Gates

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Group :01

Student’s ID : 2013-1-80-022

Student’s name :Md. Solayman Khan

**Objective Of The Experiment**:

The objective of this experiment was to learn and implement the TTL logic and observe the switching characteristics’ of logic functions by using different kind of logic gates.

**Some common fixed function logic gates:**

|  |  |
| --- | --- |
| 7400 -quad 2-input NAND gate |  |
| 7402- quad 2-input NOR gate |  |
|  7404- hex inverter |  |
|  7408- quad 2-input AND gate |  |
|  7410- triple 3-input NAND gate |  |
|  7411- triple 3-input AND gate |  |
|  7420- dual 4-input NAND gate |  |
|  7421- dual 4-input AND gate |  |
|  7427- triple 3-input NOR gate |
| 7430-8-input NAND gate |
|  7432- quad 2-input OR gate |
|  7486- quad 2-input XOR gate |

In this experiment, we have used only 7400 and 7404 IC’s.

**Diagram of IC’s:**



Figure1:Some common fixed function logic gates

**MATLAB command for Vin vs. Vout plot of Hex inverter:**

Vin=x=[0,1.26,1.32,1.38,1.45,1.5,2,2.5,3,3.5,4,4.5,5,5.5];

Vout (at Vcc=5V )=y=[3.48,0.17,0.17,0.17,0.17,0.17,0.17,0.18,0.17,0.17,0.17,0.17,0.17,0.17];

Vout (at Vcc=4.8V)=z=[3.22,0.16,0.15,0.17,0.15,0.16,0.18,0.17,0.16,0.17,0.16,0.17,0.16,0.17];

Vout (at Vcc=5.2V)=t=[3.84,0.17,0.17,0.17,0.17,0.16,0.18,0.17,0.16,0.18,0.17,0.19,0.17,0.16];

plot(x,y);

hold on

plot(x,z);

hold on

plot(x,t);

**Answer to the Report Questions**

**Answer to the Question 01**

Normally,

VH(max)=5V

VH(min)=2V

VL(max)=0.8V

VL(min)=0V

**Answer to the Question 02**



Figure2: Plot of Vin vs. Vout for Hex inverter at Vcc=5V, Vcc=4.8V,Vcc=5.2v .

**Truth table for some mostly used logic gates:**

OR : AND : NOR :

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

NAND: XOR: NOT:

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

|  |  |
| --- | --- |
| A | Output |
| 0 | 1 |
| 1 | 0 |

**Conclusion:**

 In this experiment, we have verified the Nand gate and analyzed Hex inverter. Our knowledge about logic gates has been improved due to this experiment.