**Dept. of EEE, EWU, Summer 2014**

Course Name : Digital Logic Design

Course Code : EEE205

Experiment No : 02

Name of the Experiment : Implementation of Boolean Function Using AND, OR, and

NOT Logic Gates.

Date of Performance : 20/05/2014

Date of submission : 28/05/2014

Group no. : 01

Student’s ID : 2013-1-80-022

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**Objective Of The Experiment**:

In this particular experiment, we have learned about Boolean functions briefly and also got more familiarity with different logic gate containing IC’s like 7404,7408and 7432.

**Name of the IC’s:**

1. 1 pc 7404- hex inverter
2. 2 pcs.7408- quad 2-input AND gate
3. 1 pc7432- quad 2-input OR gate

**Circuit diagrams:**

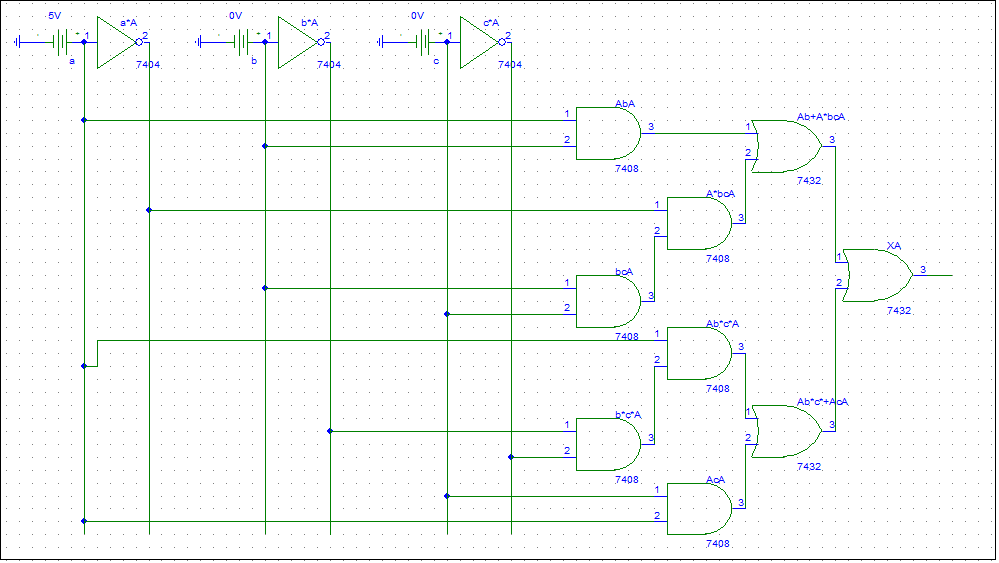
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Figure1:Diagram of the circuit for

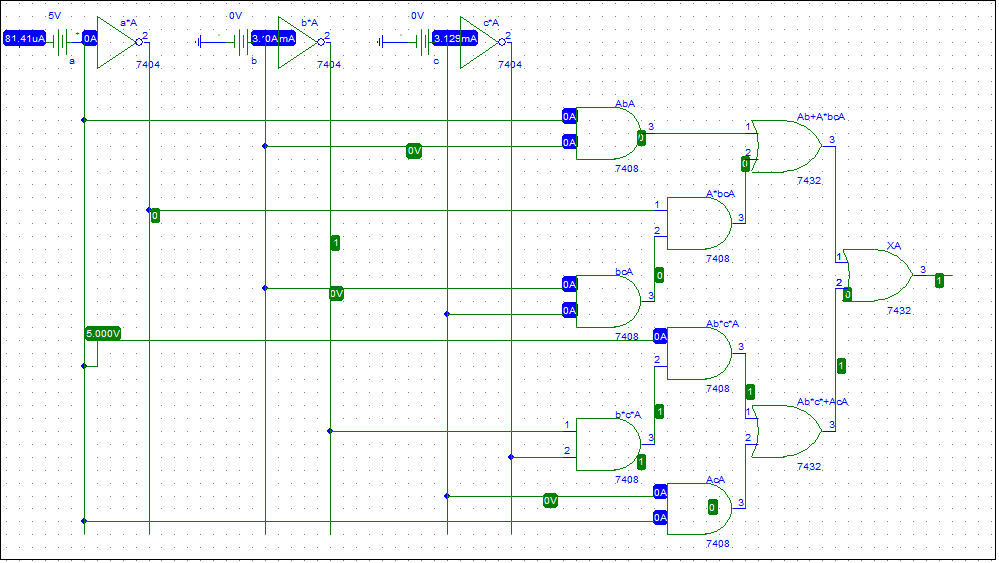


Figure2:Simulation of the circuit of figure1 at a=1,b=0,c=0

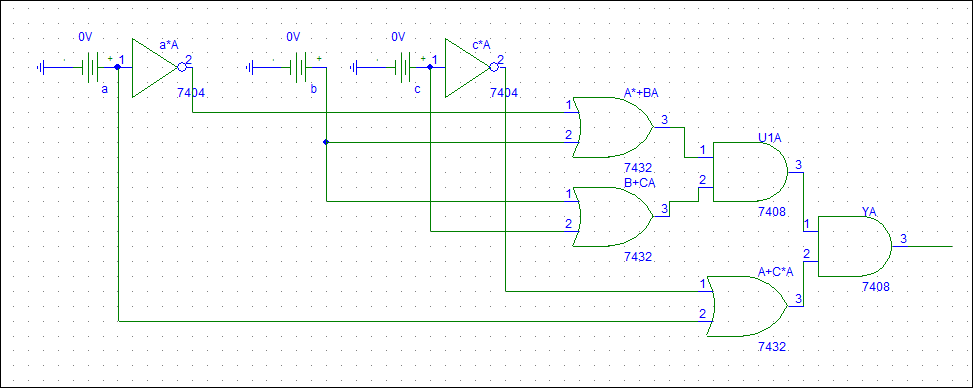
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Figure3:Diagram of the circuit for

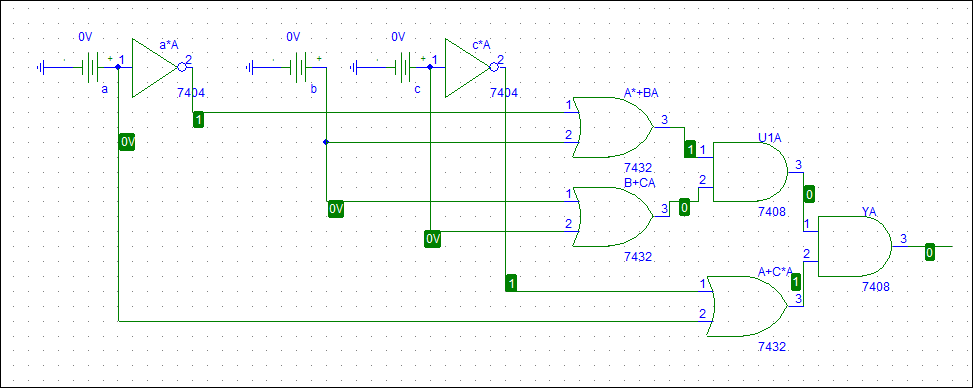
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Figure4:Simulation of the circuit of figure3 at a=0,b=0,c=0

**Answer to the Report Questions**

**Answer to the Question 01**

The truth table for is given below-

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Combinations | | | | Output |
| A | B | C |  |  |  |  | X |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

Verification: This table is completely same with the table in pre-lab.

Now,

The truth table for is given below-

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Combinations | | | Output |
| A | B | C |  |  |  | Y |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Verification: This table is also same with the table in pre-lab.

**Answer to the Question 02**

**Transforming X to standard form:**

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=

Truth table for standard form of X:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Combinations | | | | | Output |
| A | B | C |  |  |  |  |  | X |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

**Verification:** This truth table is also same with the truth table of X in pre-lab.

**Transforming Y to standard form:**

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Y=

Truth table for standard form of Y:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Combinations | | | | | Output |
| A | B | C |  |  |  |  |  | Y |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Verification:** This truth table is also same with the truth table of Y in pre-lab.

**Conclusion:**

In this experiment, we have verified the Boolean functions both of SOP and POS form.From this experiment, it is clear to us that, the output function is always same for both normal form and standard form, if there is no mistake. Our skill of transforming from SOP to POS and from POS to SOP is also sharpened through this experiment.