**Dept. of EEE, EWU, Summer 2014**

Course Name : Digital Logic Design

Course Code : EEE205

Experiment No : 07

Name of the Experiment : Designing a 4-to-16 decoder using Verilog HDL

Date of Performance : 23/07/2014

Date of submission : 06/08/2014

Group no. : 01

Student’s ID : 2013-1-80-022

Student’s name : Md. Solayman Khan

**Objective Of The Experiment**:

In this particular experiment, our main objective was to design a 2to4 decoder and to use it to build a 4 to 16 decoder. And then to use it to verify two given functions.

**Answer to the Question 01**

A decoder is just a combination of different logic gates to implement a function. Different decoders are designed in different way.

There is difference between implementing a function using decoders and multiplexer.To implement a function using decoder, we have to add external gates on the outputs of the decoder and if we want to use multiplexer to implement a function, we have to select the inputs as our required outputs.

**Conclusion:**

In this experiment, we have implemented 2 to 4 decoder using varilog. We also implemented 4 to 16 decoder by using 2 to 4 decoder by call function method. Then we implemented two functions by using the outputs of the 4 to 16 decoder.